Remarks

Applicant presented claims 1-23 for examination. The examiner has rejected claims 1-23. By this amendment, claims 1, 12-16 have been amended, and claim 17 has been canceled. Thus, claims 1-16, 18-23 remain.

Claim Rejections - 35 USC §103

The examiner rejected claims 1-23 under 35 USC 103(a) as being unpatentable over Kaneda (US Patent No. 4,400,769) in view of Bhandai (US Patent No. 6,532,533). Applicant respectfully traverses.

Before a claim by claim analysis is provided, applicant believes it would be helpful to provide a brief overview of Kaneda. Kaneda is directed to a virtual machine system, defined as a computing system in which instructions issued by a program may be different from those actually executed by the hardware to perform a given task. Col. 1, lines 18-23. A specific context of his virtual machine system is shown in Figure 2 where a real machine 11 is coupled to a virtual machine manager 22, which manages a plurality of virtual machines 20. When the virtual machines 20 execute non privileged instructions, they are passed to the virtual machine manager 22 and then to the real machine 11 for execution. However, when the virtual machines 20 desire to execute privileged instructions (i.e., kernel instructions), they are passed to the virtual machine manager 22 which interfaces to the real machine 11, and causes the virtual machine manager 22 to pass simulations of the privileged instructions to the real machine 11. Col. 3, lines 28-34. One such event which causes simulation of a privileged instruction is when an interrupt occurs to the virtual machine manager 22. The virtual machine manager 22 then carries out a process in accordance with the source of the interrupt. Col. 3, lines 63-68. Of particular interest to the examiner was the fact that Kaneda discusses a privileged instruction which is used for controlling a PSW (program status word). That is, Kaneda shows a privileged register within his real machine 11 which can be modified by a privileged operation. Moreover, Kaneda shows a modification register 53 which operates so as to modify the PSW which controls each OS. Col. 8, lines 37-43. What applicant would like the examiner to appreciate, however, is that the modification register 53 is located in the CPU (the real machine), and that these registers are not directly sensible, or

writable by the programs (or instructions) of any of the virtual machines. Col. 10, lines 1-7. That is, there is nothing in Kaneda which allows a privileged instruction (provided by either any of the virtual machines 20, or the virtual machine manager 22) to ATOMICALLY set or clear bits within a control register within the real machine 11. Applicant has reviewed Kaneda, and cannot find any indication of an instruction that can, with atomicity, set or clear bits within a control register. Applicant presumes an understanding as to why this is the case. At the time Kaneda was filed (1980), microprocessors only executed 1 instruction at a time. Such instructions begin, executed, and completed, before the next instruction begin. And, an instruction would complete before an interrupt was handled. Morever, execution of each instruction required many clock cycles. But, in today's pipelined microprocessors, many instructions are executing concurrently, within sequential or parallel stages within a microprocessor. Thus, there is the possibility of an interrupt occurring during the execution of an instruction. This problem was detailed in the present application, with particular reference to Figure 5. It is this problem that requires the novel idea of the present invention, which allows an instruction to atomically update a privileged register, and more specifically, to specify within the instruction, which bits within the privileged register are to be set or cleared atomically. The teaching of Bhandal (showing a plurality of mask registers) adds nothing to the novel atomicity, and specificity within the operands, as taught by the present instruction.

With respect to claim 1, it is repeated below for ease of reference:

1. (Currently amended) A microprocessor having a control register that is atomically modifiable by a privileged (kernel) instruction, the control register having bit fields, the microprocessor comprising:

a core, for receiving the privileged instruction and for atomically modifying the control register upon execution of the privileged instruction;

the privileged instruction comprising:

an opcode, for identifying the instruction as a privileged instruction;

a first operand, for specifying the control register as a register to be modified; and

a second operand, for specifying a location of a second register within the microprocessor, said second register containing a bit mask, said bit mask determining which of the bit fields within the control register are to be modified;

wherein said bit mask is used to atomically set or clear the bit fields in the control register;

whereby the bit fields in the control register are modified atomically by the privileged instruction.

Claim 1, as originally submitted and as amended, particularly shows a privileged instruction which has an opcode, and two operands, one for specifying a control register to be modified, and a second for specifying which bits within the control register are to be modified, atomically. As stated by the examiner, nothing in Kaneda details atomic operations. Applicant further believes that nothing in Kaneda shows a privileged instruction having an opcode, and two operands, having the structure and function specified in claim 1. Therefore, applicant believes that claim 1 is allowable over Kaneda, taken alone. The examiner indicates however that Bhandal teaches atomicity with respect to read and write instructions (Col. 1, line 57 - col. 2, line 35. Applicant traverses. What Bhandal teaches is the use of a plurality of mask registers, each dedicated to a particular function, to control which pins they mask get read or written. This allows pins on his processor to be read or written atomically, depending on which function is executing, and thus, which mask associated with that function is controlling access to the pins. Applicant makes several observations. First, Bhandal does not show a privileged instruction, which, as part of its operands, specifies at execution of the instruction, which bits are to be set or cleared within a control register, atomically. That is, in Bhandal, the

masks must have already been set to allow the atomic reading or writing to particular pins. Second, there is nothing in either Kaneda or Bhandal to suggest combining them with each other. The examiner is reminded that it is improper to combine references, in hindsight, in an attempt to reconstruct applicant's invention without some suggestion in the references for the combination. Kaneda is directed at a virtual machine. Bhandal is directed at a plurality of masks to control reads/writes to processor pins. Nothing in either is directed at a microprocessor having a privileged instruction which specifies bits within a control register to be set or cleared atomically. Thus, their combination is also not directed at this novel feature. Third, even if there was some suggestion for the combination, applicant is at a loss to understand what the combination would be. Perhaps it would be a plurality of mask registers which would control how each of the virtual machines accessed their modification registers 53? Whatever the combination would be, it certainly is not the novel invention as recited in claim 1. For all of these reasons, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 2-11, these depend from claim 1 and add further limitations which are neither anticipated nor obviated by Kaneda, taken alone or in combination with Bhandal. For all of the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claim 12, it is repeated below as amended, for ease of reference:

12. (Currently amended) A method for atomically modifying bits within a privileged control register of a microprocessor, the method comprising:

providing a privileged instruction which instructs the microprocessor to atomically clear specified ones of the bits;

providing a register, for specifying which of the particular ones of the bits are to be cleared; and

upon receipt of an interrupt by the microprocessor, atomically clearing the particular ones of the bits as specified by the register.

As in claim 1, claim 12 particularly shows a method for providing a privileged instruction which instructs a microprocessor to atomically clear specified ones of bits within a privileged control register. This is neither taught, suggest, or hinted at by Kaneda, taken alone or in combination with Bhandal. For all of the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 13-16, these depend from claim 12 and add further limitations which are neither anticipated nor obviated by Kaneda, taken alone or in combination with Bhandal. For the reasons stated above with respect to claims 1 and 12, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claim 17, it has been canceled rendering the examiner's rejection moot.

With respect to claim 18, this claim as originally presented particularly claims a privileged instruction, which specifies within its operands, which control register should be acted upon, and which bits within the control register should be cleared. Nothing in Kaneda or Bhandal is directed at this novel instruction. For all of the reasons stated above, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claim 19, it depends from 18 and adds further limitations which are neither anticipated nor obviated by Kaneda, taken alone or in combination with Bhandal. Applicant therefore respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claim 20, this claim is similar to claim 1 as originally presented. Thus, for the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 21-22, these depend from claim 20 and for the same reasons should be allowable over Kaneda taken alone or in combination with Bhandal. Applicant therefore respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claim 23, it recites structure similar to claims 1 and 20, and thus should be allowable over Kaneda taken alone or in combination with Bhandal. Applicant therefore respectfully requests the examiner to withdraw his rejection of this claim.

Applicant has reviewed the other art cited by the examiner and has not found any reference which taken alone or in combination would obviate the novel teachings of the present invention as found in the recited claims. For all of these reasons, applicant respectfully requests the examiner to remove his rejections of the pending claims and move this application forward to allowance. Of course, if the Examiner has any questions about this application, or any of the pending claims, he is encouraged to contact me directly.

Respectfully submitted,

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